Amendments to the Claims

1. (Currently amended) A semiconductor device, comprising:

a semiconductor chip;

a single dielectric layer;

electrically conductive leads on said dielectric layer; and

a low temperature curing adhesive material that cures to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit so as to avoid misalignment between said chip and said single dielectric layer, said low temperature curing adhesive material being located between said semiconductor chip and said dielectric layer.

2. (Previously presented) The semiconductor device of claim 1, wherein said single dielectric layer includes polyimide.

3. (Previously presented) The semiconductor device of claim 1, wherein said single dielectric layer includes benzocylobutene.

4. (Original) The semiconductor device of claim 1, further comprising bond wires connecting said semiconductor chip to said electrically conductive leads.

5. (Original) The semiconductor device of claim 4, further comprising resin material encapsulating said bond wires.

6. (Previously presented) The semiconductor device of claim 5, further comprising an opening defined in said single dielectric layer, and wherein said bond wires and said resin material are located in said opening.

7. (Original) The semiconductor device of claim 6, further comprising a ball grid array on said leads.

8-9. (Canceled)

10. (Currently amended) A taped semiconductor product, comprising:

integrated circuits formed in semiconductor material;

a tape having openings aligned with said integrated circuits, wherein said tape includes a single dielectric layer and electrically conductive leads, said leads being printed on said single dielectric layer;

bond wires extending through said openings, said bond wires being electrically connected to said integrated circuits; and

adhesive material between said tape and said integrated circuits, wherein said adhesive material cures to about ninety percent of its maximum strength within twenty four to thirty six hours at room temperature so as to avoid misalignment between said tape and said integrated circuits.

11. (Original) The taped semiconductor product of claim 10, further comprising glob top encapsulant material in said openings.

12. (Original) The taped semiconductor product of claim 11, further comprising a ball grid array for each of said integrated circuits, said ball grid arrays being located on said electrically conductive leads.

13. (Currently amended) A tape for semiconductor devices, said tape comprising:

a single dielectric layer having openings;

electrically conductive leads associated with said openings, said leads being printed on said dielectric layer; and

a low temperature curing adhesive material located so as to provide adhesion between a semiconductor chip and said dielectric layer, said adhesive material capable of ~~that cures~~ curing to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit so as to avoid misalignment between said chip and said dielectric layer~~, said low temperature curing adhesive material being located between a semiconductor chip and said dielectric layer~~.

14. (Previously presented) The tape of claim 13, wherein said single dielectric layer includes polyimide.

15. (Previously presented) The tape of claim 13, wherein said single dielectric layer includes benzocylobutene.

16. (Original) The tape of claim 13, wherein said dielectric material includes a metal alloy and a polymer coating.

17. (Original) The tape of claim 13, wherein said openings are slot-shaped to expose aligned bond pads.

18. (Original) The tape of claim 17, wherein said openings are punched through said dielectric layer.

19. (Withdrawn) A method of making semiconductor devices, said method comprising the steps of:

providing a semiconductor product having integrated circuits;

providing a tape having a dielectric layer and electrically conductive leads;

adhering said tape to said semiconductor product at low temperature; and

electrically connecting said integrated circuits to said electrically conductive leads.

20. (Withdrawn) The method of claim 19, wherein the temperature of said tape does not exceed one hundred fifty degrees Fahrenheit during said adhering step.

21. (Withdrawn) The method of claim 20, wherein said step of electrically connecting said integrated circuits to said leads includes the step of connecting bond wires to bond pads on said semiconductor product.

22. (Withdrawn) The method of claim 21, further comprising the step of locating ball grid arrays on said electrically conductive leads.

23. (Withdrawn) The method of claim 22, further comprising the step of encapsulating said bond wires in resin.

24. (Withdrawn) The method of claim 23, further comprising the step of dicing said semiconductor product to separate said integrated circuits into individual semiconductor chips.

25. (Withdrawn) A method of making taped products, said method comprising the steps of:

providing a sheet having electrically conductive leads and an epoxy adhesive layer;

aligning said sheet with respect to integrated circuits; and

curing said adhesive layer at low temperature.

26. (Withdrawn) The method of claim 25, further comprising the step of connecting wires to said integrated circuits and said electrically conductive leads.

27. (Withdrawn) The method of claim 26, wherein the temperature of said adhesive layer does not exceed one hundred degrees Fahrenheit during said curing step.

28. (Withdrawn) The method of claim 27, further comprising the step of connecting ball grid arrays to said leads.

29. (Withdrawn) The method of claim 28, further comprising the step of flowing resin through a mask to glob top encapsulate said wires.

30. (Withdrawn) The method of claim 29, further comprising the step of separating said integrated circuits from each other to produce integrated circuit devices.

31. (Currently amended) A semiconductor device, comprising:

a semiconductor chip;

a single dielectric layer;

electrically conductive leads on said single dielectric layer; and

an anisotropically conductive adhesive material located between said single dielectric layer and said semiconductor chip, said adhesive material capable of curing so as to avoid misalignment between said dielectric layer and said chip.

32. (Previously presented) The semiconductor device of claim 31, further comprising via holes defined in said single dielectric layer, and metal located in said via holes, said metal being connected to said leads.

33. (Original) The semiconductor device of claim 32, further comprising a ball grid array on said leads, said ball grid array being located within the periphery of said chip.

REMARKS

Reconsideration and allowance of this application, as amended, are respectfully requested. Claims 1, 10, 13, and 31 have been amended. Claims 1-7 and 10-33 remain pending in the application, with claims 19-30 withdrawn from consideration as directed to a non-elected invention.[1] The rejections are respectfully submitted to be obviated in view of the amendments and remarks presented herein.

In the Amendment, claims 1, 10, 13, and 31 have been amended to further define the claimed adhesive material (i.e., essentially as suggested by the Examiner in his telephone message of June 14, 2002). For example, claim 1 now defines a semiconductor device that includes, *inter alia*, "a low temperature curing adhesive material that cures to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit *so as to avoid misalignment between said chip and said single dielectric layer.*"

35 U.S.C. § 103(a) – Heo in view of admitted prior art

Claims 1, 2, 4-7, 10-14, and 16-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,858,815 to Heo et al. (hereinafter "Heo") in view of the admitted prior art, Master Bond Polymer System EP31 ("Master Bond").

The rejection is respectfully traversed. The Office Action has failed to establish a *prima facie* case of obviousness because all of the claimed limitations are not taught or suggested by the applied prior art references. Specifically, the asserted combination fails

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[1] The Disposition of Claims section of the Office Action Summary indicates that "[c]laims 1-7, 10-18, and 31-33 is/are pending in the application." Applicant's attorney notes, however, that all of claims 1-7 and 10-33 remain pending in the application. Although claims 19-30 have been withdrawn from consideration as directed to a non-elected invention, claims 19-30 remain pending.

to teach or suggest, *inter alia,* the claimed feature of "a low temperature curing adhesive material that cures to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit *so as to avoid misalignment between said chip and said single dielectric layer*" (claim 1). Claim 10, which defines in pertinent part an "adhesive material [that] cures to about ninety percent of its maximum strength within twenty four to thirty six hours at room temperature *so as to avoid misalignment between said tape and said integrated circuits,*" is similarly allowable. Claim 13, which defines in pertinent part "a low temperature curing adhesive material located so as to provide adhesion between a semiconductor chip and said dielectric layer, said adhesive material capable of curing to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit so as to avoid misalignment between said chip and said dielectric layer," is also allowable.

Furthermore, the combined disclosures would not have rendered obvious the embodiments of the invention defined by any of the pending claims. Regardless of what Master Bond may teach, there is no suggestion whatsoever in Heo to employ the adhesive disclosed by Master Bond. The claimed invention would not have been obvious because there is no suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to combine reference teachings to attain the claimed invention.

There is no suggestion in Heo of employing any particular adhesive material, let alone Applicant's claimed adhesive material. Heo discloses simply using "an epoxy adhesive or an adhesive film" (column 5, line 20). Applicant, however, employs the claimed low temperature curing adhesive material for a specific utility – to avoid misalignment between the structural elements joined by the adhesive (specification page 4,

lines 20-22; page 10, lines 10-13). See also specification page 4, lines 4-6, where Applicant teaches that "[t]he low temperature curing adhesive material avoids misalignment problems that would be caused by a heat activated adhesive."

Applicant respectfully submits that the rejection is based on impermissible hindsight reconstruction. The reconstruction is impermissible because it includes knowledge that was gleaned only from Applicant's disclosure. Heo discloses simply using "an epoxy adhesive or an adhesive film." There is no evidence whatsoever that Heo contemplated the potential misalignment problems described by Applicant, let alone that Heo contemplated the use of Applicant's claimed low temperature curing adhesive material as a means to avoid such misalignment.

The rejection of claims 3 and 15 is similarly traversed. Each of claims 3 and 15 depends from an independent claim that is allowable for the reasons discussed above with respect to the rejection of claims 1, 2, 4-7, 10-14, and 16-18. Chang adds nothing to rectify the deficiency associated with the asserted combination of Heo and Master Bond.

The rejection of claims 31-33 is also traversed. Applicant's claim 31 defines a semiconductor device that includes in pertinent part "an anisotropically conductive adhesive material located between said single dielectric layer and said semiconductor chip, *said adhesive material capable of curing so as to avoid misalignment between said dielectric layer and said chip*." Heo discloses an "adhesive means 30" that "comprises an epoxy adhesive or an adhesive film" (column 5, lines 18-20). Regardless of what Akagawa may disclose with regard to an insulation layer, there is no suggestion in the asserted combination of Applicant's claimed semiconductor device comprising an anisotropically conductive adhesive material.

For at least the above reasons, reconsideration and withdrawal of each of the rejections under § 103(a) are respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By _____

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